REMARKS

The present application was filed on January 23, 2004 with claims 1 through 26. Following a late restriction requirement, claims 16-21 were elected. Despite a traversal in Applicants' prior response, the Examiner has maintained the restriction requirement. Thus, Applicants have cancelled unelected claims 1-15 and 22-26, without prejudice. Claims 15 through 21 are presently pending in the above-identified patent application.

In the Office Action, the Examiner withdrew the indication of allowability of claims 16-21 and rejected claims 16 and 19 under 35 U.S.C. §103(a) as being unpatentable over Ashizawa (United States Number 6,990,034). Apparently, claims 17 and 20 were also included in this grouping. The Examiner indicated that claims 18 and 21 would be allowable if rewritten in independent form.

Independent claim 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ashizawa. The Examiner asserts that Ashizawa discloses in Figures 1 and 2, a memory device (1) where a bit line pair (BL, XBL) are precharged to a high level up to time t4 (associated with a normal operating mode), and at time t4, a precharge cancel signal changes to a high level to turn off the p-MOSFET 30.

The Examiner acknowledges that Ashizawa did not discuss a read only memory (ROM) as required by independent claim 16. Even assuming for the sake of argument that Ashizawa suggests, in the context of an SRAM, the sequence of a precharge phase followed by active (read) phase, followed by a standby phase or cycle, does not mean there is any disclosure or suggestion to apply such techniques in a ROM.

In order to establish a *prima facie* case of obviousness, the following three criteria must be met:

> [f]irst, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

M.P.E.P. §2143. Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to modify Ashizawa in the manner suggested by the Examiner.

Unlike the SRAM context of Ashizawa, ROM designs have only single-ended bitlines and the bitlines usually are connected directly to an inverter. Therefore, the bitlines in a ROM cannot float during standby as they do in Ashizawa's SRAM patent, as recognized by the Examiner on page 4, lines 3-6. An SRAM is also different in that it has differential bitline pairs. Unlike SRAM, conventional ROM designs keep the bitlines at precharge at the end of the cycle in standby, therefore ready for the active phase of the next Read cycle.

The ROMs of the present invention, however, precharge at least one column in the ROM during a precharge phase of each read cycle, but the at least one column is **not** precharged during a standby phase. Rather, in an exemplary embodiment, the bitline is held, for example, at ground during the standby phase. This holding of the bitline at ground saves power.

Thus, a person of ordinary skill in the art would not look to the SRAM techniques of Ashizawa to solve the ROM problems solved by the present invention.

Independent claim 16 emphasizes that the precharge phase techniques of the present invention are applied in a ROM.

Applicants respectfully request the withdrawal of the rejection of independent claim 16.

Dependent Claims

Claims 16, 17, 19 and 20 are dependent on independent claim 16 and and are therefore patentably distinguished over Ashizawa because of their dependency from independent claim 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

The Examiner indicated that claims 18 and 21 would be allowable if rewritten in independent form.

It is respectfully submitted that all of the pending claims, i.e., claims 16-21, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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